ABSTRACT

A clock generator generates a first clock signal and a second clock signal such that the timing of the first and second clock signals is adjustable. A phase detector is coupled to receive the first and second clock signals and generate a skip signal by integrating the first clock signal over one half of a clock cycle. The skip signal indicates whether the first clock signal is ahead of the second clock signal. The first and second clock signals are calibrated individually. The skip signal generated by the phase detector indicates whether a load pulse should be sampled.